Remarks

Applicant respectfully requests reconsideration of this application as amended. Claims 13, 14, 20, 21, 26, and 27 have been amended. No claims have been cancelled or added. Therefore, claims 13-31 are presented for examination.

35 U.S.C. §103(a) Rejection

Claims 13-31 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Tsuyoshi et al. (U.S. Patent No.4,949,325) in further view of Inada et al. (U.S. Patent No. 5,534,807). Applicant submits that the present claims are patentable over Tsuyoshi in view of Inada.

Tsuyoshi discloses a method of recording/reproducing information associated with an apparatus and recording medium. The medium has an alternate formation including tracks of first regions wherein at least an optical record of formatted pits at a constant time interval is recorded and second regions in which information is recorded so that optical retrieval can be achieved. A clock signal is generated based on the readout signal of the preformatted pits to record an information signal in the second regions, and the clock signal is retarded and used to read out data pits that are the record of the information in the second regions. (Tsuyoshi at Abstract.)

Inada discloses a sampling circuit that is not susceptible to an influence of structural components and environmental changes. The circuit includes a phase difference detecting circuit that detects a deviation of a sampling clock from optimal sampling timing and outputs a phase difference signal. On the other hand, a phase reference signal that is used as a reference to determine a phase advance and a phase lag is generated by a phase reference

detecting circuit. In accordance with these signals, a sampling clock shifting circuit shifts the sampling clock so that the sampling clock is activated at optimal sampling time. (Inada at Abstract.)

Claim 13, as amended, recites:

> A method for recovering a digital data signal (D_{out}) and a clock signal (Ck_{out}) comprising:
> receiving a data signal (D_{in}) including a plurality of successive bits;
> generating, from the data signal (D_{in}), the clock signal (Ck_{out}) with a resonator circuit;
> delaying the data signal (D_{in}) to compensate for a delay created by the generating the clock signal (Ck_{out}) so that the data signal (D_{in}) is synchronized with the clock signal (Ck_{out});
> phase locking the clock signal (Ck_{out}) to the delayed data signal by measuring via a phase detector a phase difference between the clock signal (Ck_{out}) and the delayed data signal and by time delaying the clock signal (Ck_{out}) based on the phase difference, wherein measuring the phase difference includes sampling in the phase detector the delayed data signal with the clock signal (Ck_{out}) in three flip-flops at three different points in time;
> sampling the delayed data signal at approximately the center of each bit with the delayed clock signal (Ck_{out}); and
> generating, as a result of the sampling, the digital data signal (D_{out}).

Applicant submits that Tsuyoshi does not disclose or suggest delaying the data signal (D_{in}) to compensate for a delay created by the generating the clock signal (Ck_{out}) so that the data signal (D_{in}) is synchronized with the clock signal (Ck_{out}) and phase locking the clock signal (Ck_{out}) to the delayed data signal by measuring via a phase detector a phase difference between the clock signal (Ck_{out}) and the delayed data signal and by time delaying the clock signal (Ck_{out}) based on the phase difference, as recited by claim 13. Applicant submits that Tsuyoshi does not disclose ***both of*** delaying a data signal to compensate for a delay created by generating the clock signal and then phase locking the clock signal to the data signal. While Tsuyoshi may disclose delaying the data signal to compensate for a delay created by generating a clock signal, Tsuyoshi does not then also disclose phase locking the data signal

to the clock signal. Therefore, Tsuyoshi does not disclose or suggest the cited features of claim 13.

Applicant further submits that Inada does not disclose or suggest delaying the data signal (D_{in}) to compensate for a delay created by the generating the clock signal (Ck_{out}) so that the data signal (D_{in}) is synchronized with the clock signal (Ck_{out}) and phase locking the clock signal (Ck_{out}) to the delayed data signal by measuring via a phase detector a phase difference between the clock signal (Ck_{out}) and the delayed data signal and by time delaying the clock signal (Ck_{out}) based on the phase difference. The Final Office Action does not rely on Inada to disclose these features and applicant can find no disclosure or suggestion anywhere in Inada of either of these features. Therefore, Inada does not disclose or suggest the cited features of claim 13.

As neither Tsuyoshi or Inada individually disclose delaying the data signal (D_{in}) to compensate for a delay created by the generating the clock signal (Ck_{out}) so that the data signal (D_{in}) is synchronized with the clock signal (Ck_{out}) and phase locking the clock signal (Ck_{out}) to the delayed data signal by measuring via a phase detector a phase difference between the clock signal (Ck_{out}) and the delayed data signal and by time delaying the clock signal (Ck_{out}) based on the phase difference, any combination of Tsuyoshi and Inada also does not disclose or suggest such a feature. Therefore, claim 13, as well as its dependent claims, it patentable over Tsuyoshi in view of Inada.

Independent claims 20 and 26 also recite, in part, delaying the data signal (D_{in}) to compensate for a delay created by the generating the clock signal (Ck_{out}) so that the data signal (D_{in}) is synchronized with the clock signal (Ck_{out}) and phase locking the clock signal (Ck_{out}) to the delayed data signal by measuring via a phase detector a phase difference

between the clock signal (Ck_{out}) and the delayed data signal and by time delaying the clock signal (Ck_{out}) based on the phase difference. As discussed above, Tsuyoshi in view of Inada does not disclose or suggest such a feature. Therefore, claims 20 and 26 are patentable over Tsuyoshi in view of Inada for the reasons discussed above with respect to claim 13.

Applicant respectfully submits that the rejections have been overcome and that the claims are in condition for allowance. Accordingly, applicant respectfully requests the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Applicant respectfully petitions for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17(a) for such an extension.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

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